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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/774,441 | 02/10/2004 | Dae-Ning Guo | BHT-3111-413 | 8831 |

7590 10/18/2006

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| EXAMINER | |
|---|---|
| LE, DIEU-MINH T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2114 | |

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/774,441 | GUO ET AL. | |
| | Examiner | Art Unit | |
| | Dieu-Minh Le | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

1. This Office Action is response to the communication filed on 02/10/04 in application 10/774,441.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stenfort (US. 6,662,334) in view of Kuslak et al. (US. 7,093,190 hereafter referred to as Kuslak).

As per claim 1:

Stenfort substantially teach the invention. Stenfort teaches:

- A method for accessing data from a storage medium according to requirements of a host, the storage medium storing a plurality of data blocks (i.e., ***data sector***), wherein each of the data blocks comprises a plurality of data sectors and an error correction code (ECC) for recovering errors of the each of the data blocks, and each of the data sectors comprises an error detection code (EDC) [i.e., ***EDAC, error detection and correction***, col. 4, lines 17-18] for detecting correctness of the each of the data sectors, the method [abstract, col. 1, lines 9-12 and col. 3, lines 50 through col. 4, lines 12]; comprising steps of:
- fetching a data block from the data blocks of the storage medium [col. 3, lines 50 through col. 4, lines 12 and col. 4, lines 50-53];
- recovering errors of the data block by the ECC of the data block [col. 3, lines 50 through col. 4, lines 12 and col. 4, lines 50-53];
- detecting correctness of each data sector of the data block by the EDC of the each data sector of the data block [col. 3, lines 50 through col. 4, lines 12 and col. 4, lines 53-55].
- performing (i.e., ***performing error detection and correction***) following sub-steps when at least one incorrect

data sector is detected [col. 3, lines 50 through col. 4, lines 12 and col. 4, lines 50-53];
- storing correct data sectors of the data block [col. 3, lines 50 through col. 4, lines 12 and col. 4, lines 55-60];
- overwriting data [col. 3, lines 50 through col. 4, lines 12 and col. 4, lines 66 through col. 5, lines 4];

Stenfort does not explicitly address:
- re-fetching and re-performing data.

However, Stenfort does disclose capability of:
- A method and device for performing error detection and correction on EDAC data sector in data storage medium [abstract, fig. 2, col. 6, lines 61 through col. 7, lines 29] comprising:
- ***a "repeating" process for data receiving (i.e., re-fetching and re-performing), data detecting, data storing, etc…***[col. 3, lines 50 through col. 4, lines 11] as well as ***data read/write pointers including wrapping back functionality*** [col. 10, lines 45 through col. 11, lines 15].

In addition, Kuslak explicitly teaches:
- A system and method for handling parity error in a data processing via data storage device [abstract, col. 1, lines 7-11] comprising:
- ***fetching and re-fetching data within data storage locations for its execution processes*** [fig. 4, col. 3, lines 8-22 and col. 10, lines 58 through col. 11, lines 43].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Stenfort's ***a "repeating" process for data receiving (i.e., re-fetching and re-performing), data detecting, data storing, etc…*** as well as ***data read/write pointers including wrapping back functionality*** as being the re-fetching and re-performing data as claimed by Applicant. This is because Stenfort's detection and correction on EDAC data sector in data storage medium explicitly performed data monitoring, detecting, executing, decoding via its ***repeating fetching and re-performing*** processes. By utilizing these capabilities, the operating processing within the computing memory system, more specifically the data storage access, can be directed/re-directed or configured properly via its data fetching, executing, and storing, based upon its error condition response and determination in supporting the EDAC operation; second, by applying the ***fetching and re-fetching data within data storage locations for its execution processes*** as taught by Kuslak in conjunction with the method and device for performing error detection and correction on EDAC data sector in data storage medium as taught by Stenfort, the data memory system within digital computing system can enhance its operation performance, more specifically to ensuring the error detected, corrected, in proper and efficient manner via its re-fetching and re-performing processes.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the digital data memory computing system operation availability and network/system performance therein with a mechanism to enhance the data memory access, data debugging,

data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 2-4:

Stenfort further teaches:

- wherein the storage medium is accessed by one of a CD-ROM drive, a DVD-ROM drive, a DVD player and a DVD.+-.RW drive [col. 2, lines 36-49];
- wherein the ECC comprises outer-code parity (PO) data and inner-code parity (PI) data encoded in a form of Reed Solomon Product Code (RSPC) [col. 1, 41-50];
- transferring the data block to the host when all the data sectors of the data block are correct [fig. 3, col. 7, lines 65 through col. 8, lines 65 and col. 9, lines 5-10].

In addition, Kuslak explicitly teaches:

- A method for handling a ***parity error*** in a data processing system, comprising: a.) receiving a parity error while retrieving data signals stored within a storage location of a first storage device; b.) determining whether a predetermined number of parity errors occurred during prior operations performed to the first storage location; c.) recording the existence of the parity error and continuing to use the storage location if the predetermined number of ***parity errors*** did not occur during the prior operations; and d.) discontinuing use of the storage location if the predetermined number of parity errors did occur during the prior operations [col. 11, lines 54-67].

As per claims 5-6:

Stenfort further teaches:

- storing the correct data sectors in a specific memory block having a location different with that of the data block is stored [col. 4, lines 7-12];

Stenfort does not explicitly address:

- re-fetching the data block to store the re-fetched data block into a same location of a memory occupied by the previously fetched data block.

However, Stenfort does disclose capability of:

- A method and device for performing error detection and correction on EDAC data sector in data storage medium [abstract, fig. 2, col. 6, lines 61 through col. 7, lines 29] comprising:

- ***a "repeating" process for data receiving (i.e., re-fetching and re-performing), data detecting, data storing, etc…*** [col. 3, lines 50 through col. 4, lines 11] as well as ***data read/write pointers including wrapping back functionality*** [col. 10, lines 45 through col. 11, lines 15].

In addition, Kuslak explicitly teaches:

- A system and method for handling parity error in a data processing via data storage device [abstract, col. 1, lines 7-11] comprising:

- ***fetching and re-fetching data within data storage locations for its execution processes*** [fig. 4, col. 3,

lines 8-22 and col. 10, lines 58 through col. 11, lines 43].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Stenfort's ***a "repeating" process for data receiving (i.e., re-fetching and re-performing), data detecting, data storing, etc…*** as well as ***data read/write pointers including wrapping back functionality*** as being the re-fetching the data block to store the re-fetched data block into a same location of a memory occupied by the previously fetched data block as claimed by Applicant. This is because Stenfort's detection and correction on EDAC data sector in data storage medium explicitly performed data monitoring, detecting, executing, decoding via its ***repeating fetching and wrapping*** processes within in memory location. By utilizing these capabilities, the operating processing within the computing memory system, more specifically the data storage access, can be directed/re-directed or configured properly via its data fetching, executing, and storing within in memory location; second, by applying the ***re-fetching data within data storage locations for its execution processes*** as taught by Kuslak in conjunction with the method and device for performing error detection and correction on EDAC data sector in data storage medium as taught by Stenfort, the data memory system within digital computing system can enhance its operation performance, more specifically to ensuring the error detected, corrected, in proper and efficient manner for the same reasons set forth as described in claim 1, **supra**.

As per claims 7-13:

Due to the similarity of claims 7-13 to claims 1-6; therefore, these claims are also rejected under the same rationale applied against claims 1-6. **In addition, all of the limitations have been noted in the rejection as per claims** 1-6. Such as, ***an optical electronic system is explicitly disclosed by Stenfort*** [col. 12, lines 24-25].

As per claims 14-19:

These claims are similar to claims 1-6. The only minor different is that these claims introduce "a first and second memory blocks" instead of a plurality data blocks as described in claim 1. However, Stenfort explicitly disclosed a ***plurality of data areas and sectors (i.e., blocks) within storage memory device used for performing error detection and correction on EDAC data sector in data storage medium*** [col. 8, lines 12-17 and col. 9, lines 56-67]; therefore, these claims are also rejected under the same rationale applied against claims 1-6. **In addition, all of the limitations have been noted in the rejection as per claims** 1-6. Such as, ***an optical electronic system is explicitly disclosed by Stenfort*** [col. 12, lines 24-25].

## ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this

letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**DIEU-MINH THAI LE**
**PRIMARY EXAMINER**
**ART UNIT 2114**

DML
10/15/06